Graphene Field-Effect Transistors with Gigahertz-Frequency Power Gain on Flexible Substrates

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ABSTRACT: The development of flexible electronics operating at radio-frequencies (RF) requires materials that combine excellent electronic performance and the ability to withstand high levels of strain. In this work, we fabricate graphene field-effect transistors (GFETs) on flexible substrates from graphene grown by chemical vapor deposition (CVD). Our devices demonstrate unity-current-gain frequencies, \( f_T \), and unity-power-gain frequencies, \( f_{\text{max}} \), up to 10.7 GHz and 3.7 GHz, respectively, with strain limits of 1.75%. These devices represent the only reported technology to achieve gigahertz-frequency power gain at strain levels above 0.5%. As such, they demonstrate the potential of CVD graphene to enable a broad range of flexible electronic technologies which require both high flexibility and RF operation.

KEYWORDS: Graphene, CVD, flexible, radio frequency, FET

The field of flexible electronics has been active for more than 15 years, driven by the desire for low-cost, large-area, pliable electronics for such applications as e-paper, flexible displays, chemical and biological sensors, and smart tags. The electronic materials used in these cases have largely been polymers and small-molecule organic films because of the desire to exploit large-area, low-cost fabrication approaches, such as roll-to-roll dry3 or inkjet printing. The resulting electronic device performance, however, has been relatively poor, with inherent low-field mobilities typically less than 1 cm² V⁻¹ s⁻¹ and mobilities in integrated devices typically below 0.05 cm² V⁻¹ s⁻¹.¹⁻³ Both reliability and low-voltage operation have been challenging. In addition, it is important for any proposed flexible technology to maintain uniform electronic properties over a wide range of strain, \( \varepsilon \), which is related to the thickness, \( t \), and bending radius, \( \rho \), of the substrate as \( \varepsilon = t/(2\rho) \).

The desire to improve the performance of these devices has led to growing efforts to transfer wires, ribbons, and membranes of traditional semiconducting materials to flexible substrates. Materials such as silicon nanomembranes (SiNMs),¹⁻⁷ III–V metal–oxide–semiconductor thin films⁴ and nanowires,⁹ indium–gallium–zinc–oxide,¹⁰ and AlGaN/GaN heterostructures¹¹ have been investigated, as have carbon nanotubes (CNTs)¹²⁻¹⁵ and graphene.¹⁶,¹⁷ However, enhancements to electronic performance have been achieved at the expense of device flexibility; to date, no flexible technology has achieved both unity-current-gain frequencies, \( f_T \), and unity-power-gain frequencies, \( f_{\text{max}} \), in the GHz regime at strains above 0.5%. CNT devices have demonstrated \( f_T \) performance approaching 1 GHz at 1% strain for 0.8 \( \mu \)m channel lengths.¹²,¹³ However, \( f_{\text{max}} \), which is far more important for circuit applications, is not reported. In fact, \( f_{\text{max}} \) is expected to be substantially less than \( f_T \), following similar trends for field-effect transistors (FETs) based on mats of CNTs on rigid substrates.¹⁸ The highest values of \( f_{\text{max}} \) for FETs fabricated on flexible substrates have been reported for SiNMs⁵ and III–V metal–oxide–semiconductor thin films⁶ at 12 GHz and 23 GHz, respectively. However, FETs based on these bulk semiconductor materials all exhibit strain limits below 0.5%.⁴,⁵,⁸,¹¹

Graphene’s unique electronic¹⁹,²⁰ and mechanical²¹ properties make it a promising material for the fabrication of FETs which require both high flexibility and high operating frequencies. While graphene has no band gap, rendering it poorly suited for digital applications, its high carrier mobility,¹⁹,²² saturation velocity,²³⁻²⁵ and current-carrying capacity²⁶,²⁷ make it a promising candidate for high-frequency analog applications. Graphene-based FETs (GFETs) fabricated on rigid substrates have in fact demonstrated values of \( f_{\text{max}} \) of up to 34 GHz at channel lengths of 600 nm.²⁸

Methods for producing graphene films suitable for flexible electronics include dielectrophoretic deposition of solution-processed graphene¹⁶ and large-area growth of graphene by chemical vapor deposition (CVD).²⁹ GFETs from solution-processed methods demonstrate \( f_T \) performance of approximately 2.2 GHz at a 170 nm channel length under strain up to 0.5%.³⁰ However, poor electrostatics in these devices result in nonsaturating current–voltage (\( I–V \)) characteristics and \( f_{\text{max}} \) values of only 550 MHz.³⁰ In contrast, CVD graphene films display excellent electronic properties comparable to those of exfoliated graphene.³⁰ Even on flexible substrates, GFETs fabricated from CVD graphene exhibit field-effect mobilities up to 4900 cm² V⁻¹ s⁻¹ and maintain stable DC electronic properties at high levels of strain.³²⁻³⁷ In this work we demonstrate GFETs fabricated from CVD graphene with \( f_{\text{max}} \).

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of 3.7 GHz (at channel lengths of 500 nm) and strain limits of 1.75%. Figure 1 compares the work presented here with other flexible high-frequency technologies on the merits of \( f_{\text{max}} \) and strain limits, showing that the GFETs fabricated in this work are the first transistors to attain power gain in the GHz regime at strains above 0.5%.

Figure 2a shows a schematic of the GFETs fabricated in this work. A bottom-gated device structure is implemented, motivated by previous work demonstrating that bottom-gated fabrication of GFETs with a dielectric layer applied over the gate electrode yields higher performance than top-gated devices which attempt to grow a gate oxide on the graphene surface.\(^{28,38}\) GFETs are fabricated on 127 \( \mu \)m thick polyethylene naphthalate (PEN) substrates (DuPont Teijin Films). Two-fingered bottom-gates (1 nm Ti/30 nm Au−Pd alloy) are defined by electron beam lithography and lift-off. The contact pad region of the gate is further thickened by subsequent patterning and evaporation of Ti/Au (1 nm/50 nm). A 6-nm gate dielectric of HfO\(_2\) is conformally grown by atomic layer deposition (ALD) at 150 °C yielding a dielectric constant of \( \kappa \approx 13.39\) Large, single-crystals of graphene are grown by chemical vapor deposition (CVD) and transferred over the gate using well-established procedures.\(^{30}\) Graphene is patterned with a second lithography step and reactive ion etching in an oxygen plasma. The devices are completed by evaporating Ti/Pd/Au (1 nm/15 nm/50 nm) source and drain electrodes to contact the graphene. Devices are left uncapped. In addition, the thermal limits of the polymer substrate (~180 °C) prevent high-temperature thermal annealing processes from being used to remove resist residue on the graphene channel. Figure 2b shows a cross-sectional schematic of a completed device. GFETs are fabricated with a gate length of 500 nm, source-to-drain spacing of 900 nm, and an effective channel width of 30 \( \mu \)m (two 15-\( \mu \)m wide gates in parallel). Figure 2c shows an optical micrograph of a GFET device fabricated on a PEN substrate.

Electronic device characteristics are measured under ambient conditions. Samples are strained during electronic measurements by applying uniaxial tensile strain in the y-direction (see Figure 2c) under two-point bending conditions, as shown in Figure 2d. The strain, \( \varepsilon_{yy} \), is calculated from the bending geometry using elastaic theory assuming frictionless end supports.\(^{40}\) Flexible GFET DC performance in the linear transport region is shown in Figure 3a−c, where the device resistance, \( R \), is displayed against gate-to-source voltage, \( V_{\text{gs}} \), taken with fixed source-to-drain voltage (\( V_{\text{sd}} = 10 \text{ mV} \)) at increasing strain from \( \varepsilon_{yy} = 0\% \) to 1.75%. Low-bias field-effect mobility, \( \mu_{\text{FE}} \), is calculated from \( \mu_{\text{FE}} = (L_{\text{ch}}/W_{\text{ch}})(V_{\text{sd}} C_{\text{tot}} V_{\text{gs}}) \), where \( L_{\text{ch}} \) is the channel length, \( W_{\text{ch}} \) is the channel width, \( C_{\text{tot}} \) is the total effective gate capacitance per unit area, and \( V_{\text{gs}} \) is the small-signal transconductance, defined as \( (\partial I_d/\partial V_{\text{gs}})_{V_{\text{sd}}} \), where \( I_d \) is the measured drain current. \( C_{\text{tot}} \) is determined by the series combination of the electrostatic capacitance, \( C' \), and the
quantum capacitance, $C_q$. For the devices presented in this work, $C_q \approx 1700 \text{nF cm}^{-2}$, based on a parallel plate model. $C_q$ is density-dependent over the charge carrier density range pertinent to this work ($n = 0.5-10 \times 10^{12} \text{ cm}^{-2}$), but it can be approximated as the mean of $C_q$ values calculated over this carrier density range. This approach, shown to be valid for similar devices over an equivalent carrier density range, yields a constant value of $C_q \approx 2000 \text{nF cm}^{-2}$. These values of $C_q$ and $C_r$ result in $C_{rd} \approx 919 \text{nF cm}^{-2}$. The source-to-gate current, $I_{sg}$, is measured to remain below 0.5 pA over the entire strain range during device characterization, indicating negligible leakage current through the dielectric even at high strain. $I_{sg}$ for our flexible GFET is $\sim 1500 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ (for $V_{gs} = -0.25 \text{ V}$, the gate bias that yields the maximum $g_{m}$ for this device). This mobility is comparable to similar devices fabricated from exfoliated graphene on silicon substrates, demonstrating the excellent electronic quality of the CVD graphene utilized in this work. Although mobility remains relatively constant with strain up to $\varepsilon_{yy} = 1.75\%$, the position of the Dirac point with respect to $V_{gs}$ is observed to shift with increasing strain. We attribute this shift to changes in device electrostatics, related to mobile trapped charges in the gate oxide and at the graphene–oxide interface, as the substrate is flexed. The presence of trapped charges in the gate oxide, at the graphene–oxide interface, or in resist residue on the graphene surface additionally accounts for the hysteresis in the position of the Dirac point with respect to $V_{gs}$ ($\sim 0.5 \text{ V}$) observed in low-bias measurements. We note, however, that the presence of residual resist residue from lithographic processing does not significantly contribute to the contact resistance between the graphene channel and evaporated electrodes, as the total contact resistance for this device is less than 300 $\Omega \ \mu\text{m}$, in the range best contact resistances reported for GFET devices ($200-1000 \Omega \ \mu\text{m}$). The ungated regions of the graphene channel will, however, effectively increase the contact resistance of the device. Improvements to the device architecture which act to minimize the gate-to-source and gate-to-drain spacer regions, such as by utilizing a self-aligned fabrication scheme, can further reduce the effective channel resistance.

Figure 3d–f shows $I-V$ characteristics for the same representative device, with $I_{sd}$ plotted as a function of $V_{sd}$ at values of $V_{gs}$ decreasing from 0.25 V to $-1 \text{ V}$ in 0.25 V steps. Device characteristics represent a unipolar p-channel device. Devices are only measured up to $V_{sd} = 0.5 \text{ V}$ due to the thermal limitations of the polymer substrate. Above $V_{sd} = 0.5 \text{ V}$ the substrate melts locally under the device channel, causing both the substrate and overlaying GFET to mechanically warp in structure. $I-V$ characteristics are plotted for increasing levels of strain ranging from 0% to 1.75%. Changes in $I_f$ with increasing strain are correlated to the observed shifts in the Dirac point in Figure 2a–c. At $\varepsilon_{yy} = 0\%$, measured values of $g_{m}$ and output resistance, $r_0$, are 5.1 m$\Omega$ and 259 $\Omega$, respectively, at a bias point of $V_{gs} = -0.25 \text{ V}$ and $V_{sd} = 0.5 \text{ V}$. We observe a maximum current density of 0.28 mA/$\mu\text{m}$, consistent with values reported for devices fabricated from CVD graphene of similar structure at equivalent electric fields.

Figure 4 shows RF characteristics for this same GFET device characterized in Figure 3. Both current-gain ($h_{21}$) and unilateral power gain ($U$) are extracted from S-parameters measured at...

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**Figure 3.** (a–c) Low-field transport characteristics of a flexible GFET with a device channel width of 30 $\mu\text{m}$. Device resistance, $R$, is plotted against gate-to-source voltage, $V_{gs}$, at a fixed source-to-drain bias of $V_{sd} = 10 \text{ mV}$. (d–f) Current–voltage ($I-V$) characteristics plotting drain current, $I_{ds}$, as a function of $V_{sd}$. $I-V$ curves are taken at fixed $V_{gs}$ decreasing from 0.25 V (orange) to $-1 \text{ V}$ (black) in 0.25 V steps. Data are presented for increasing values of strain of $\varepsilon_{yy} = 0\%$ (a,d), $\varepsilon_{yy} = 1.25\%$ (b,e), and $\varepsilon_{yy} = 1.75\%$ (c,f).

**Figure 4.** High-frequency device characteristics, current gain ($h_{21}$) and unilateral power gain ($U$), plotted as a function of frequency (without de-embedding). High-frequency characteristics are presented for strain values of $\varepsilon_{yy} = 0\%$ (a), $\varepsilon_{yy} = 1.25\%$ (b), and $\varepsilon_{yy} = 1.75\%$ (c). Values of extrinsic $f_T$ and $f_{max}$ are calculated for each strain state. Measurements are performed at a fixed source-to-drain voltage, $V_{sd} = 0.5 \text{ V}$ and gate-to-source voltages, $V_{gs}$ of $-0.25 \text{ V}$ (a), 0.4 V (b), and 0.6 V (c). The dashed line is a guide to the eye with a $-20 \text{ dB/decade}$ slope, included to demonstrate that devices follow well this expected frequency dependence.
of strain. Both $g_m$ (Figure 5a) and $r_o$ (Figure 5b) exhibit low variance (less than $\pm25\%$) up to strains of $\epsilon_{yy} = 1.1\%$. At strains greater than $1.1\%$, variations in $r_o$ increase up to $\pm40\%$, likely related to the observed shifts in device electrostatics (most notably the shift in the Dirac point) with flexure. Figure 5c plots device gate capacitance extracted directly from measured device electrostatics, $C_{gg}$, as a function of strain. We note that the value of $C_{gg}$ extracted at $\epsilon_{yy} = 0\%$ is $941 \text{ nF cm}^{-2}$, which matches well the expected value for $C_{tot}$ of $919 \text{ nF cm}^{-2}$ as described before. The variation in $C_{gg}$ with strain is likely attributed to the change in trapped charges. Accounting for observed variations in $C_{gg}$ with strain, values of $\mu_{FE}$ at strains above $\epsilon_{yy} = 0\%$ are calculated utilizing $C_{gg}$ values extracted at equivalent strain states. Mobility for the device remains uniform with device flexure (Figure 5d), exhibiting less than $\pm30\%$ variance across the entire measured strain range up to $\epsilon_{yy} = 1.75\%$, in good agreement with previous theoretical calculations and experimental observations, demonstrating the stability of the intrinsic electronic properties of the CVD graphene channel. Figure 5e plots cutoff frequency as a function of strain. In all cases, $V_{dd}$ is $0.5 \text{ V}$, and $V_{gs}$ is chosen at each measured strain point to maximize the device transconductance; these values of $V_{gs}$ are also shown in Figure 5e. Both $f_T$ and $f_{max}$ demonstrate low variance (less than $\pm20\%$) with strain up to $\epsilon_{yy} = 1.1\%$, above which an increase in both $f_T$ and $f_{max}$ of up to $40\%$ is observed. We note that both DC and RF performance of the device remain uniform up to strains of $\epsilon_{yy} = 1.1\%$; improvements to device structure which reduce trapped charges can allow for improved uniformity of electronic properties at strains greater than $\epsilon_{yy} = 1.1\%$. Above strains of $\epsilon_{yy} = 1.75\%$, most devices begin to fail as a result of cracking of the gate electrode, corresponding to clear irreversible degradations in electronic characteristics.

In conclusion, we demonstrate flexible GFETs fabricated from CVD graphene which display extrinsic values of $f_T$ and $f_{max}$ up to $10.7 \text{ GHz}$ and $3.7 \text{ GHz}$, respectively, with strain limits of $1.75\%$. This is the first example of a flexible technology exhibiting both gigahertz-frequency power gain and strain limits above $0.5\%$. As such, this work demonstrates the potential of CVD graphene as a material to enable a wide-range of highly flexible electronic technologies requiring analog FETs operating in the gigahertz frequency range.

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Notes

The authors declare no competing financial interest.

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