On-chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS

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Abstract

An on-chip transistor characterization system for combined C-V/I-V characterization is presented. Capacitance measurement uses a quasi-static charged-based measurement technique with atto-Farad resolution. Random and systematic variability in device I-V and C-V characteristics is studied. The random variability in intrinsic gate capacitance is shown to exhibit Pelgrom scaling. Correlation between I-V and C-V measurements is used to identify systematic channel-length variation gradients in a device array.

Introduction

With variability in transistor characteristics steadily increasing with each new technology node, there is a growing need for integrated device characterization of large device sample sets. Prior work has focused on ring oscillator [1] or SRAM-based test structures [2,3], integrating circuit-specific arrays for characterization. In this work, we present a fully integrated on-chip quasi-static device characterization system with digital interfaces for combined capacitance-voltage (C-V) and current-voltage (I-V) characterization in 45-nm CMOS. Large addressable device-under-test (DUT) arrays allow us to gather statistically significant data across different device geometries and full on-chip integration enables us to improve sampling speeds for high data throughput; digital interfaces make the system compatible with a digital test flow. Random and systematic variability in the I-V and C-V characteristics and C-V/I-V correlation is studied.

On-Chip Characterization System

Fig. 1 shows the top-level view of the on-chip characterization system (a die photo of the 5-mm-by-5-mm chip is shown in inset) as implemented in a 45-nm bulk CMOS process. An on-chip switching matrix addresses one of nearly 2200 nFETs of 28 different sizes and configurations. A four-channel, eight-bit R-string DAC is used to bias the DUT; 256-bit bi-directional shift registers control the DAC outputs in a one-hot fashion. The DAC can operate at sampling rates of up to 1 MHz and has an LSB of 5 mV. Current- and voltage-mode ADCs can be routed through the switching matrix to each of the DUT terminals enabling accurate four-point Kelvin measurements. The voltage-mode ADC has a sampling rate of 100 kHz for an LSB of 0.7 mV. The current-mode ADC has a sampling rate of 100 kHz for an LSB of 5 nA when operated in I-V mode (I_{REF} = 5 μA), and a sampling rate of 1 kHz for an LSB of 244 pA when operated in C-V mode (I_{REF} = 500 nA).

Both ADCs operate as dual-slope integrators and are based around the same integrator core (**Fig. 2**). A thick-oxide MOS capacitor is used as the integrating element, making the design compatible with a digital CMOS process. A two-stage opamp is implemented by cascading a folded-cascode input stage with a common-source output stage. A gain of 90 dB enables 14-bit conversion accuracy, while < 500 Ω output impedance ensures the ability to drive large DUTs. A 14-bit counter is implemented using native 45-nm devices and is clocked at 1.8 GHz, allowing us to achieve 14-bit resolution at a 100 kHz sampling rate.

Measurement Techniques

In this work, we perform dc I-V and quasi-static C-V device characterization on the same nominal size device. I-V characterization is implemented using Kelvin sensing (**Fig. 3**). C-V characterization is implemented using a leakage-insensitive charge-based capacitance measurement (CBCM) technique (**Fig. 4**) discussed in detail below. Standard CBCM techniques have been used in the past for interconnect characterization [4] and device characterization [5]. In this work, integration allows higher resolution in current (and capacitance), and implementation at an aggressive technology node requires careful handling of leakage currents.

The proposed atto-Farad-resolution, leakage-insensitive CBCM technique is illustrated in **Fig. 4**. For the DUTs considered here, V_G is set to 1.5 V and V_C is swept from 0.2 V to 1.5 V in increments, ΔV, of 5 mV. The gate current measured during the discharge phase of the clock, $I_{G,D}$, is divided by the clock frequency, f_{CLK}, to derive the charge profile, Q_G, which is then differentiated with respect to V_C to derive the gate-to-channel capacitance, C_{GC}. It should be noted that since the bias conditions during the discharge cycle are always the same (gate biased at V_G and source/drain shorted to ground), any errors due to leakage and charge-injection result in a constant offset, $Q_{G,0}$, which is cancelled out during differentiation (**Fig. 5**). A 51-point second-order Savitzky-Golay polynomial interpolation filter is implemented to compute the numerical derivatives used in the capacitance derivation.

Measurement Results

Measurements discussed in this work focus on a sample set consisting of 15 populations of 78 nominally identical thin-oxide devices (two adjacent DUT columns with 39 devices each), spanning the space of drawn widths W_D = 0.2, 0.4, 0.6, 0.8, and 1.0 μm, and drawn lengths L_D = 0.04, 0.08, 0.11 μm. **Fig. 6** shows Kelvin-compensated constellation plots of I_D vs. V_{GS} for V_{DS} = 50 mV. **Fig. 7** shows the corresponding gate capacitance measurements, C_{GC} vs. V_{GC}.

As a representative random variability study, **Fig. 8** shows Pelgrom plots of $\sigma(\Delta V_{T,LIN})$ extracted from the I-V curves in **Fig. 6**, and $\sigma(\Delta C_{INT,ON}/C_{INT,ON})$ extracted from the C-V curves in **Fig. 7**, where $C_{INT,ON}$ is the intrinsic gate on-capacitance defined as the difference between C_{GC} at high and low gate bias. Both plots show an increased proportionality constant for minimum-length devices consistent with an effective length correction $L_{EFF} = L_D - dL$, with dL = 0.015 μm. In this case, our ability to simultaneously study the I-V and C-V characteristics of the device allows us to corroborate the results of each of the two measurements.

With respect to the systematic variations across the die, **Fig. 9** shows the normalized $C_{INT,ON}$ and $I_{D,ON}$ (defined as I_D at 0.3 V overdrive gate bias) across the entire DUT array. The two sets of data exhibit a weak negative correlation (ρ = -0.34). However, if we consider the gradients along the two columns with the largest area DUT (W/L = 1.0/0.11 μm), a much stronger negative correlation (**Fig. 10**) is observed (ρ = -0.83). Since $C_{INT,ON}$ is proportional to WLC_{OX}' and $I_{D,ON}$ is proportional to $C_{OX}'W/L$, where C_{OX}' is defined as the oxide capacitance per unit area, the observed negative correlation suggests a systematic channel-length variation along the die. This is more pronounced for larger area devices, since those exhibit less random variability in uncorrelated parameters, such as channel mobility (μ_C), which have an effect on $I_{D,ON}$, but not on $C_{INT,ON}$. The well-defined gradient in **Fig. 9b** points to the fact that systematic L variations dominate the variability in $C_{INT,ON}$. At the same time, the lack of a similarly well-defined gradient in **Fig. 9a** suggests that variations in μ_C potentially play a more significant role in overall $I_{D,ON}$ variability than L variations.

Acknowledgements

The authors would like to acknowledge TI for chip fabrication, and the Semiconductor Research Corporation for funding and support.

References:

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[3] G. Zheng, et al, *IEEE JSSC*, pp. 3174-3192, Nov. 2009.
[4] N. Arora and L. Song, *IEEE EDL*, pp. 92-94, Feb. 2004.
[5] H. Zhao, et al, *IEEE TED*, pp. 1157-1159, May 2009.

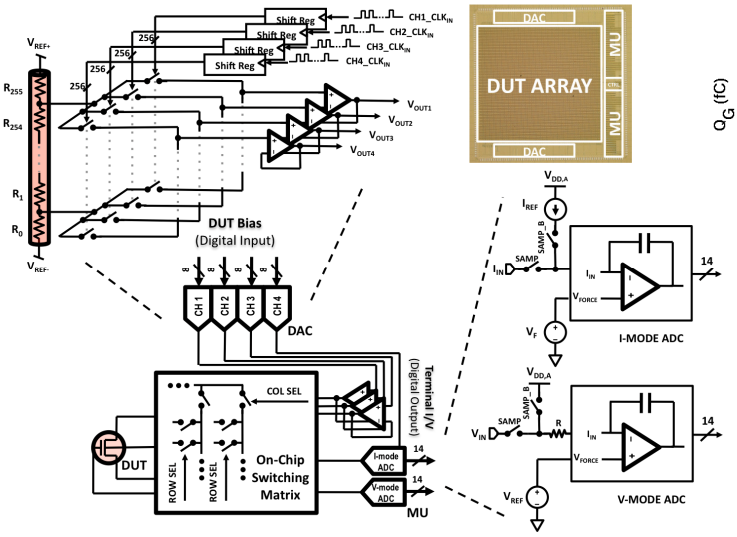


Figure 1. On-chip characterization system and die photo (inset)

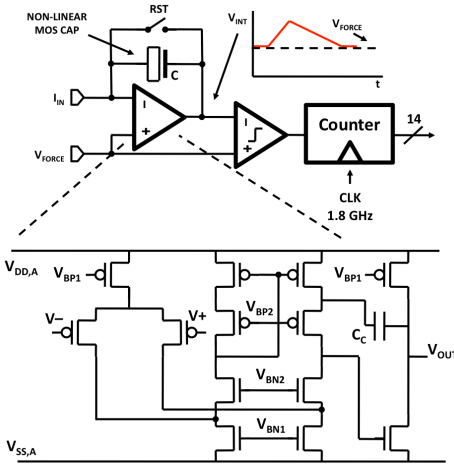


Figure 2. Dual-slope integrator core used in current-mode and voltage more ADCs; it should be noted that capacitor non-linearity does not affect the linearity of the converter, which operates on the principle of charge conservation

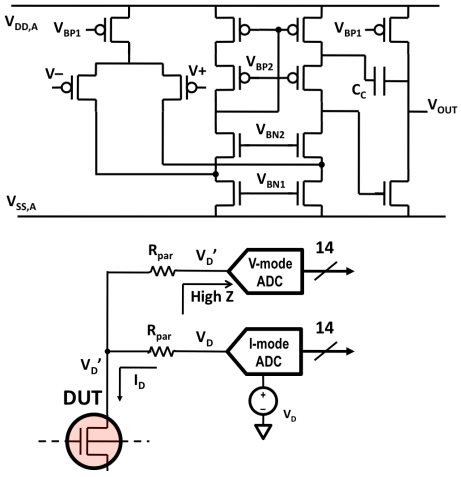
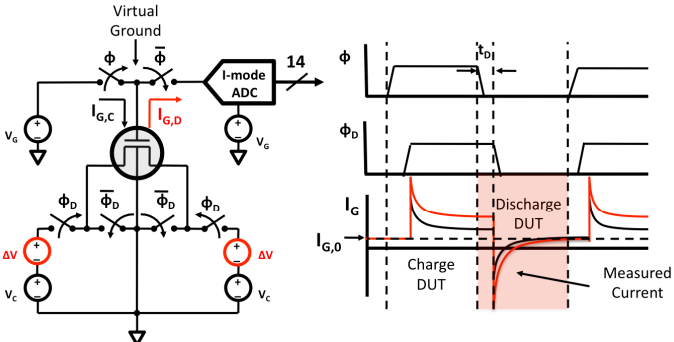


Figure 3. Four-point Kelvin measurements used to compensate parasitic resistance in the on-chip switching matrix



$$C_{GC} \equiv -\frac{\partial Q_G}{\partial V_C} \approx -\frac{\Delta Q_G}{\Delta V_C} = -\frac{\Delta I_{G,D}}{f_{CLK}\Delta V_C} = -\frac{I_{G,D2} + I_{G,0} - I_{G,D1} - I_{G,0}}{f_{CLK}(V_{C1} - V_{C2})}$$

Figure 4. Proposed leakage-insensitive on-chip CBCM technique; systematic errors due to leakage and charge-injection are accumulated only during the interval t_D < 100 ps, resulting in accuracy equivalent to that of > 5 GHz standard measurement

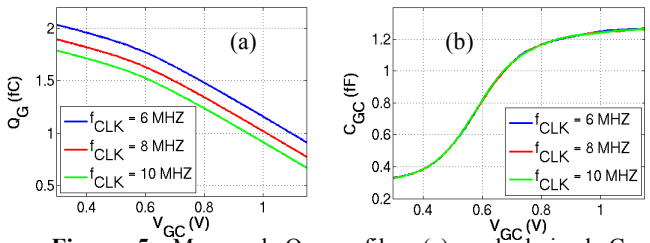


Figure 5. Measured Q_G profiles (a) and derived C_{GC} measurements (b) for three different clock frequencies (6, 8 and 10 MHz); slowing down the clock increases the constant offset in (a), but has no effect on the derived capacitance

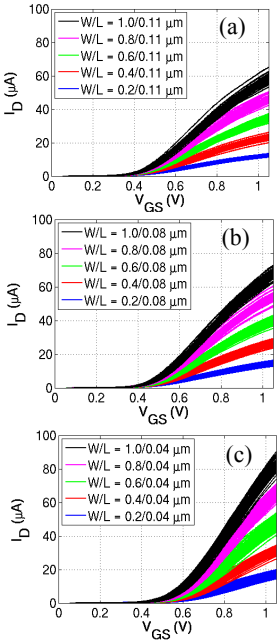


Figure 6. I_D as a function of V_{GS} for V_{DS} = 50 mV

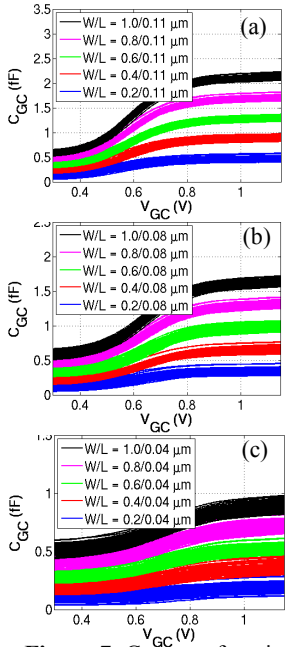


Figure 7. C_{GC} as a function of V_{GC}; C_{GC} scales with area as expected

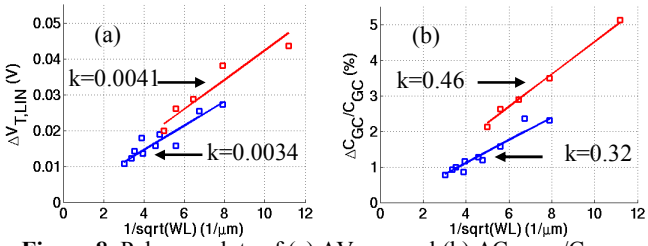


Figure 8. Pelgrom plots of (a) $\Delta V_{T,LIN}$ and (b) $\Delta C_{INT,ON}/C_{INT,ON}$; minimum-length devices (red) exhibit a higher proportionality constant (k) in both cases consistent with a decreased L_{EFF}

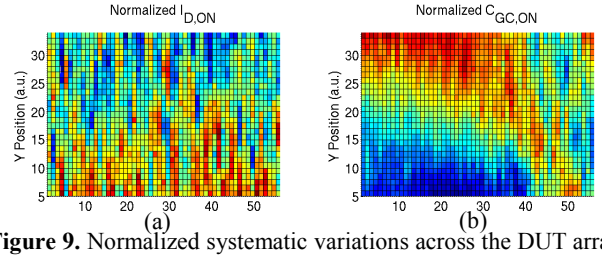


Figure 9. Normalized systematic variations across the DUT array of (a) $I_{D,ON}$ and (b) $C_{GC,ON}$; a nine-point smoothing filter has been applied to suppress the high-frequency random variations.

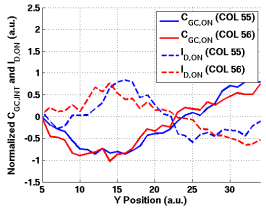


Figure 10. Strong negative correlation (ρ = -0.83) between normalized $I_{D,ON}$ and $C_{GC,ON}$ measured for the largest DUT (W/L = 1.0/0.11 µm) along the length of both array columns