On-chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS
Simeon Realov and K. L. Shepard, Department of Electrical Engineering, Columbia University
Columbia University, New York, NY 10027, (212) 854-3105, srealov@ee.columbia.edu

The proposed atto-Farad-resolution, leakage-insensitive CBCM technique is illustrated in Fig. 4. For the DUTs considered here, $V_G$ is set to 1.5 V and $V_C$ is swept from 0.2 V to 1.5 V in increments, $\Delta V$, of 5 mV. The gate current measured during the discharge phase of the clock, $I_{G,D}$, is divided by the clock frequency, $f_{CLK}$, to derive the charge profile, $Q_G$, which is then differentiated with respect to $V_C$ to derive the gate-to-channel capacitance, $C_{GC}$. It should be noted that since the bias conditions during the discharge cycle are always the same (gate biased at $V_G$ and source/drain shorted to ground), any errors due to leakage and charge-injection result in a constant offset, $Q_{G,D}$, which is cancelled out during differentiation (Fig. 5). A 51-point second-order Savitzky-Golay polynomial interpolation filter is implemented to compute the numerical derivatives used in the capacitance derivation.

Measurement Results
Measurements discussed in this work focus on a sample set consisting of 15 populations of 78 nominally identical thin-oxide devices (two adjacent DUT columns with 39 devices each), spanning the range of drawn widths $W_D = 0.2, 0.4, 0.6, 0.8,$ and $1.0 \mu m$, and drawn lengths $L_D = 0.04, 0.08, 0.11 \mu m$. Fig. 6 shows Kelvin-compensated constellation plots of $I_D$ vs. $V_{DS}$ for $V_{DS} = 50$ mV. Fig. 7 shows the corresponding gate capacitance measurements, $C_{GC}$ vs. $V_{GC}$. As a representative random variability study, Fig. 8 shows Pelgrum plots of $\sigma(\Delta V_{T,ON})$ extracted from the I-V curves in Fig. 6, and $\sigma(\Delta C_{INT,ON}/C_{INT,ON})$ extracted from the C-V curves in Fig. 7, where $C_{INT,ON}$ is the intrinsic gate on-capacitance defined as the difference between $C_{GC}$ at high and low gate bias. Both plots show an increased proportionality constant for minimum-length devices consistent with an effective length correction $I_{EFF} = L_D - dL$, with $dL = 0.015 \mu m$. In this case, our ability to simultaneously study the I-V and C-V characteristics of the device allows us to corroborate the results of each of the two measurements.

With respect to the systematic variations across the die, Fig. 9 shows the normalized $C_{INT,ON}$ and $I_{D,ON}$ (defined as $I_D$ at 0.3 V overdrive gate bias) across the entire DUT array. The two sets of data exhibit a weak negative correlation ($\rho = -0.34$). However, if we consider the gradients along the two columns with the largest area DUT ($W/L = 1.0/0.11 \mu m$), a much stronger negative correlation (Fig. 10) is observed ($\rho = -0.83$). Since $C_{INT,ON}$ is proportional to $W/L_{COX}'$ and $I_{D,ON}$ is proportional to $C_{COX}'W/L$, where $C_{COX}'$ is defined as the oxide capacitance per unit area, the observed negative correlation suggests a systematic channel-length variation along the die. This is more pronounced for larger area devices, since those exhibit less random variability in uncorrelated parameters, such as channel mobility ($\mu_C$), which have an effect on $I_{D,ON}$, but not on $C_{INT,ON}$. The well-defined gradient in Fig. 9b points to the fact that systematic L variations dominate the variability in $C_{INT,ON}$ at the same time, the lack of a similarly well-defined gradient in Fig. 9a suggests that variations in $\mu_C$ potentially play a more significant role in overall $I_{D,ON}$ variability than L variations.

Acknowledgements
The authors would like to acknowledge TI for chip fabrication, and the Semiconductor Research Corporation for funding and support.

References:
Figure 1. On-chip characterization system and die photo (inset)

Figure 2. Dual-slope integrator core used in current-mode and voltage more ADCs; it should be noted that capacitor non-linearity does not affect the linearity of the converter, which operates on the principle of charge conservation

Figure 3. Four-point Kelvin measurements used to compensate parasitic resistance in the on-chip switching matrix

Figure 4. Proposed leakage-insensitive on-chip CBCM technique; systematic errors due to leakage and charge-injection are accumulated only during the interval $t_0 < 100$ ps, resulting in accuracy equivalent to that of > 5 GHz standard measurement

Figure 5. Measured $Q_G$ profiles (a) and derived $C_{GC}$ measurements (b) for three different clock frequencies (6, 8 and 10 MHz); slowing down the clock increases the constant offset in (a), but has no effect on the derived capacitance

Figure 6. $I_D$ as a function of $V_{DS}$ for $V_{DS} = 50$ mV

Figure 7. $C_{GC}$ as a function of $V_{GC}$; $C_{GC}$ scales with area as expected

Figure 8. Pelgrom plots of (a) $\Delta V_{T,LIN}$ and (b) $\Delta C_{INT,ON}/C_{INT,ON}$; minimum-length devices (red) exhibit a higher proportionality constant ($k$) in both cases consistent with a decreased $L_{EFF}$

Figure 9. Normalized systematic variations across the DUT array of (a) $I_{D,ON}$ and (b) $C_{GC,ON}$, a nine-point smoothing filter has been applied to suppress the high-frequency random variations

Figure 10. Strong negative correlation ($\rho = -0.83$) between normalized $I_{D,ON}$ and $C_{GC,ON}$ measured for the largest DUT (W/L = 1.0/0.11 µm) along the length of both array columns